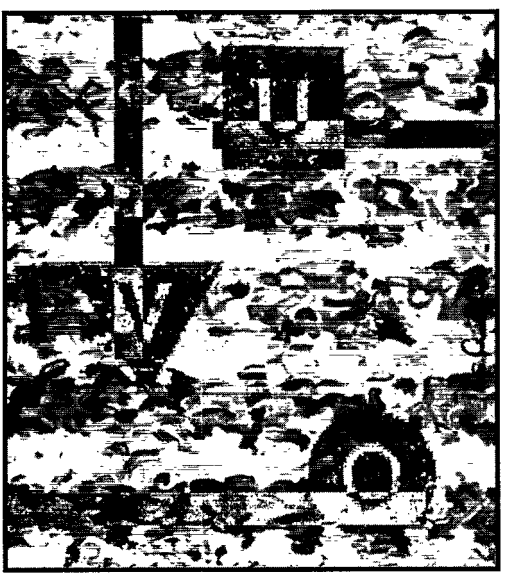
SA14-2093-00
(IBM Order Number)

MPCPRGREF/D
(Motorola Order Number)

PowerPC™ Microprocessor Family: The Programmer's Pocket Reference Guide



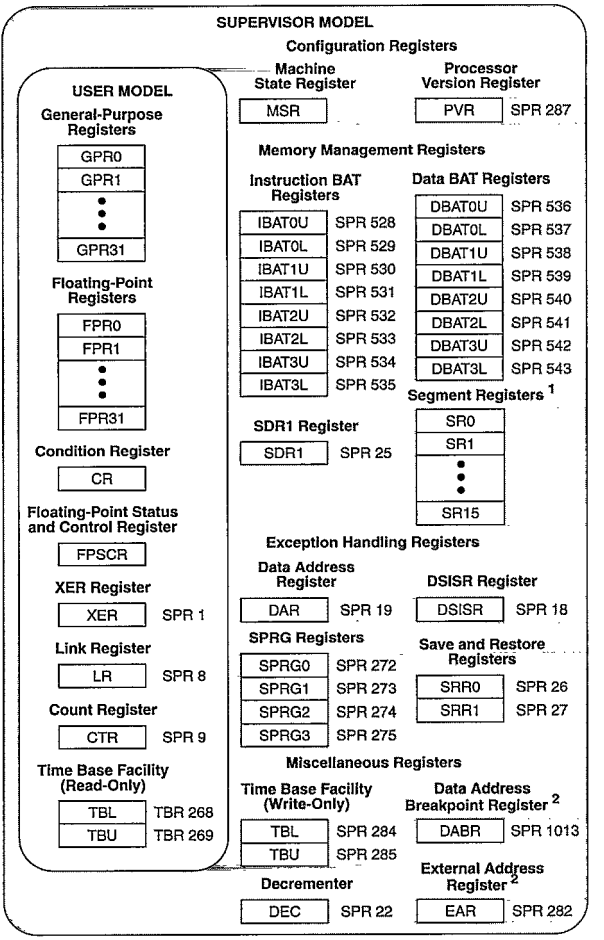
IBM. PowerPC MOTOROLA

Introduction

This document provides an overview of the PowerPC™ registers, instructions, and exceptions for 32-bit implementations. A more detailed account of the following topics or the PowerPC architecture in general, may be obtained from the *PowerPC Microprocessor Family: The Programming Environments User's Manual*, referred to as *The Programming Environments Manual* (Motorola order number MPCFPE/AD and IBM order number MPRPPCFPE-02). For further information, refer to *The PowerPC Architecture: A Specification for a New Family of RISC Processors* which remains the defining document for the PowerPC architecture.

This document contains information on the following topics:

- PowerPC programming model–registers
- Memory management registers
- Encodings for the branch options field
- MSR bit settings
- Floating-point exception mode bits
- State of MSR at power-up
- BAT register bit/field definitions and area lengths
- Segment register bit definitions and instructions
- PTE bit definitions
- Exceptions and conditions
- PowerPC instruction set



1 These registers are in 32-bit implementations only.
2 These registers are optional in the PowerPC architecture.

PowerPC Programming Model

Segment Register Bit Definition for Page Address Translation

Bit(s)	Name	Description
0	T	T = 0 selects this format
1	Ks	Supervisor-state protection key
2	Kp	User-state protection key
3	N	No-execute protection bit
4–7	—	Reserved
8–31	VSID	Virtual segment ID

Segment Register Bit Definitions for Direct-Store Segments

Bit(s)	Name	Description
0	T	T = 1 selects this format.
1	Ks	Supervisor-state protection key
2	Kp	User-state protection key
3–11	BUID	Bus unit ID
12–31	—	Device specific data for I/O controller

PTE Bit Definitions

Word	Bit(s)	Name	Description
0	0	V	Entry valid (V = 1) or invalid (V = 0)
	1–24	VSID	Virtual segment ID
	25	H	Hash function identifier
	26–31	API	Abbreviated page index
1	0–19	RPN	Physical page number
	20–22	—	Reserved
	23	R	Referenced bit
	24	C	Changed bit
	25–28	WIMG	Memory/cache control bits
	29	—	Reserved
	30–31	PP	Page protection bits

Exceptions and Conditions

Exception Type	Vector Offset (hex)	Causing Conditions
Reserved	00000	—
System reset	00100	The causes of system reset exceptions are implementation-dependent.
Machine check	00200	The causes for machine check exceptions are implementation-dependent, but typically these causes are related to conditions such as bus parity errors or attempting to access an invalid physical address.
DSI	00300	A DSI exception occurs when a data memory access cannot be performed.
ISI	00400	An ISI exception occurs when an instruction fetch cannot be performed.
External interrupt	00500	An external interrupt is generated only when an external exception is pending (typically signaled by a signal defined by the implementation) and the interrupt is enabled (MSR[EE] = 1).
Alignment	00600	An alignment exception may occur when the processor cannot perform a memory access because of alignment or endian reasons.
Program	00700	A program exception is caused by conditions which correspond to bit settings in SRR1 and arise during execution of an instruction.
Floating-point unavailable	00800	A floating-point unavailable exception is caused by an attempt to execute a floating-point instruction (including floating-point load, store, and move instructions) when the floating-point available bit is cleared, MSR[FP] = 0.
Decrementer	00900	The decrementer interrupt exception is taken if the interrupt is enabled and the exception is pending. The exception is created when the most significant bit changes from 0 to 1. If it is not enabled, the exception remains pending until it is taken.
Reserved	00A00	Reserved for implementation-specific exceptions.
Reserved	00B00	—
System call	00C00	A system call exception occurs when a System Call (**sc**) instruction is executed.
Trace	00D00	The trace exception is optional. It occurs if either the MSR[SE] = 1 and any instruction (except **rfi**) successfully completed or MSR[BE] = 1 and a branch instruction is completed.
Floating-point assist	00E00	The floating-point assist exception is optional. This exception can be used to provide software assistance for infrequent and complex floating-point operations such as denormalization.
Reserved	00E10–00FFF	—
Reserved	01000–02FFF	Reserved for implementation-specific exceptions.

Name	0	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
fnmsubsx	59	D						A					B					C								30	Rc
fresx [4]	59	D						00000					B					00000								24	Rc
frspx	63	D						00000					B					12									Rc
frsqrtex [4]	63	D						00000					B					00000								26	Rc
fselx [4]	63	D						A					B					C								23	Rc
fsqrtx [4]	63	D						00000					B					00000								22	Rc
fsqrtsx [4]	59	D						00000					B					00000								22	Rc
fsubx	63	D						A					B					00000								20	Rc
fsubsx	59	D						A					B					00000								20	Rc
icbi	31	00000						A					B					982									0
isync	19	00000						00000					00000					150									0
lbz	34	D						A					d														
lbzu	35	D						A					d														
lbzux	31	D						A					B					119									0
lbzx	31	D						A					B					87									0
lfd	50	D						A					d														
lfdu	51	D						A					d														
lfdux	31	D						A					B					631									0
lfdx	31	D						A					B					599									0
lfs	48	D						A					d														
lfsu	49	D						A					d														
lfsux	31	D						A					B					567									0
lfsx	31	D						A					B					535									0
lha	42	D						A					d														
lhau	43	D						A					d														
lhaux	31	D						A					B					375									0
lhax	31	D						A					B					343									0
lhbrx	31	D						A					B					790									0
lhz	40	D						A					d														
lhzu	41	D						A					d														
lhzux	31	D						A					B					311									0
lhzx	31	D						A					B					279									0
lmw [3]	46	D						A					d														
lswi [3]	31	D						A					NB					597									0
lswx [3]	31	D						A					B					533									0
lwarx	31	D						A					B					20									0
lwbrx	31	D						A					B					534									0
lwz	32	D						A					d														
lwzu	33	D						A					d														
lwzux	31	D						A					B					55									0
lwzx	31	D						A					B					23									0
mcrf	19	crfD		00				crfS		00			00000					0									0
mcrfs	63	crfD		00				crfS		00			00000					64									0
mcrxr	31	crfD		00				00000					00000					512									0
mfcr	31	D						00000					00000					19									0
mffsx	63	D						00000					00000					583									Rc
mfmsr [1]	31	D						00000					00000					83									0
mfspr [2]	31	D						spr										339									0
mfsr [1,5]	31	D					0	SR					00000					595									0
mfsrin [1,5]	31	D						00000					B					659									0
mftb	31	D						tbr										371									0
mtcrf	31	S					0	CRM									0	144									0
mtfsb0x	63	crbD						00000					00000					70									Rc
mtfsb1x	63	crbD						00000					00000					38									Rc
mtfsfx	63	0	FM									0	B					711									Rc
mtfsfix	63	crfD		00				00000					IMM				0	134									Rc
mtmsr [1]	31	S						00000					00000					146									0
mtspr [2]	31	S						spr										467									0
mtsr [1,5]	31	S					0	SR					00000					210									0
mtsrin [1,5]	31	S						00000					B					242									0
mulhwx	31	D						A					B				0	75									Rc
mulhwux	31	D						A					B				0	11									Rc
mulli	7	D						A					SIMM														
mullwx	31	D						A					B				OE	235									Rc
nandx	31	S						A					B					476									Rc
negx	31	D						A					00000				OE	104									Rc
norx	31	S						A					B					124									Rc
orx	31	S						A					B					444									Rc

PowerPC

Quick Reference Guide

32-Bit Implementations

Quick Reference Guide—32-Bit Implementations

Reserved

Number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	Name
	GPR*n*																																GPR*n*
	CR0				CR1				CR2				CR3			CR4					CR5				CR6				CR7				CR
	FX	FEX	VX	OX	UX	ZX	XX	VXSNAN	VXISI	VXIDI	VXZDZ	VXIMZ	VXVC	FR	FI	FPRF					0	VXSOFT	VXSQRT	VXCVI	VE	OE	UE	ZE	XE	NI	RN		FPSCR
	0000000000000												POW	0	ILE	EE	PR	FP	ME	FE0	SE	BE	FE1	0	IP	IR	DR	00			RI	LE	MSR
	T	Ks	Kp	N	0000				VSID																								SR*n*[T = 0]
	T	Ks	Kp	BUID					Controller-Specific Information																								SR*n*[T = 1]
SPR 1	SO	OV	CA	0000000000000000000000000000																					Byte Count								XER
SPR 8	Branch Address																																LR
SPR 9	CTR																																CTR
SPR 18	DSISR																																DSISR
SPR 19	DAR																																DAR
SPR 22	DEC																																DEC
SPR 25	HTABORG																				0000000								HTABMASK				SDR1
SPR 26	SRR0																														00		SRR0
SPR 27	SRR1																																SRR1
SPR 272	SPRG*n*																																SPRG*n*
SPR 282	E	0000000000000000000000000000																											RID				EAR
SPR 284	TB(L)																																TB(L) [2]
SPR 285	TBU																																TBU [2]
SPR 287	Version																				Revision												PVR
SPR 528	BEPI															0000					BL										Vs	Vp	xBAT*n*U [3]
SPR 529	BRPN																				0000000000							WIMG		0	PP		xBAT*n*L [3]
SPR 1013	DAB																														BT	DW	DR	DABR
TBR 268	TB(L)																																TB(L) [4]
TBR 269	TBU																																TBU [4]
	V	VSID																							H	API							PTE (word 0)
	RPN																					000			R	C	WIMG			0	PP		PTE (word 1)
Number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	Name

Notes: 1. Refer to *The Programming Environments Manual* for additional SPR numbers. 2. Write-Only 3. Refer to the the section concerning the memory managemantregisters for BAT register SPR numbers. 4. Read-Only

PowerPC Instruction List Sorted by Mnemonic

This table lists the instructions implemented in the PowerPC architecture in alphabetical order by mnemonic.

Name	0	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
addx	31	D					A					B				OE	266										Rc
addcx	31	D					A					B				OE	10										Rc
addex	31	D					A					B				OE	138										Rc
addi	14	D					A					SIMM															
addic	12	D					A					SIMM															
addic.	13	D					A					SIMM															
addis	15	D					A					SIMM															
addmex	31	D					A					00000				OE	234										Rc
addzex	31	D					A					00000				OE	202										Rc
andx	31	S					A					B					28										Rc
andcx	31	S					A					B					60										Rc
andi.	28	S					A					UIMM															
andis.	29	S					A					UIMM															
bx	18	LI																								AA	LK
bcx	16	BO					BI					BD														AA	LK
bcctrx	19	BO					BI					00000					528										LK
bclrx	19	BO					BI					00000					16										LK
cmp	31	crfD			0	L	A					B					0										0
cmpi	11	crfD			0	L	A					SIMM															
cmpl	31	crfD			0	L	A					B					32										0
cmpli	10	crfD			0	L	A					UIMM															
cntlzwx	31	S					A					00000					26										Rc
crand	19	crbD					crbA					crbB					257										0
crandc	19	crbD					crbA					crbB					129										0
creqv	19	crbD					crbA					crbB					289										0
crnand	19	crbD					crbA					crbB					225										0
crnor	19	crbD					crbA					crbB					33										0
cror	19	crbD					crbA					crbB					449										0
crorc	19	crbD					crbA					crbB					417										0
crxor	19	crbD					crbA					crbB					193										0
dcbf	31	00000					A					B					86										0
dcbi [1]	31	00000					A					B					470										0
dcbst	31	00000					A					B					54										0
dcbt	31	00000					A					B					278										0
dcbtst	31	00000					A					B					246										0
dcbz	31	00000					A					B					1014										0
divwx	31	D					A					B				OE	491										Rc
divwux	31	D					A					B				OE	459										Rc
eciwx	31	D					A					B					310										0
ecowx	31	S					A					B					438										0
eieio	31	00000					00000					00000					854										0
eqvx	31	S					A					B					284										Rc
extsbx	31	S					A					00000					954										Rc
extshx	31	S					A					00000					922										Rc
fabsx	63	D					00000					B					264										Rc
faddx	63	D					A					B					00000					21					Rc
faddsx	59	D					A					B					00000					21					Rc
fcmpo	63	crfD			00		A					B					32										0
fcmpu	63	crfD			00		A					B					0										0
fctiwx	63	D					00000					B					14										Rc
fctiwzx	63	D					00000					B					15										Rc
fdivx	63	D					A					B					00000					18					Rc
fdivsx	59	D					A					B					00000					18					Rc
fmaddx	63	D					A					B					C					29					Rc
fmaddsx	59	D					A					B					C					29					Rc
fmrx	63	D					00000					B					72										Rc
fmsubx	63	D					A					B					C					28					Rc
fmsubsx	59	D					A					B					C					28					Rc
fmulx	63	D					A					00000					C					25					Rc
fmulsx	59	D					A					00000					C					25					Rc
fnabsx	63	D					00000					B					136										Rc
fnegx	63	D					00000					B					40										Rc
fnmaddx	63	D					A					B					C					31					Rc
fnmaddsx	59	D					A					B					C					31					Rc
fnmsubx	63	D					A					B					C					30					Rc

MSR Bit Settings (Continued)

Bit(s)	Name	Description
23	FE1	Floating-point exception mode 1
24	—	Reserved. Full function.
25	IP	Exception prefix. The setting of this bit specifies whether an exception vector offset is prepended with Fs or 0s. In the following description, *nnnnn* is the offset of the exception. 0 Exceptions are vectored to the physical address 0x000*n_nnnn* in 32-bit implementations and 0x0000_0000_000*n_nnnn* in 64-bit implementations. 1 Exceptions are vectored to the physical address 0xFFF*n_nnnn* in 32-bit implementations and 0xFFFF_FFFF_FFF*n_nnnn* in 64-bit implementations.
26	IR	Instruction address translation 0 Instruction address translation is disabled. 1 Instruction address translation is enabled.
27	DR	Data address translation 0 Data address translation is disabled. 1 Data address translation is enabled.
28–29	—	Reserved. Full function.
30	RI	Recoverable exception (for system reset and machine check exceptions). 0 Exception is not recoverable. 1 Exception is recoverable.
31	LE	Little-endian mode enable 0 The processor runs in big-endian mode. 1 The processor runs in little-endian mode.

Note: Full function reserved bits are saved in SRR1 when an exception occurs; partial function reserved bits are not saved.

Floating-Point Exception Mode Bits

FE0	FE1	Mode
0	0	Floating-point exceptions disabled
0	1	Floating-point imprecise nonrecoverable
1	0	Floating-point imprecise recoverable
1	1	Floating-point precise mode

State of MSR at Power Up

Bit(s)	Name	Description	Bit(s)	Name	Description
0–12	—	Unspecified[1]	22	BE	0
13	POW	0	23	FE1	0
14	—	Unspecified[1]	24	—	Unspecified[1]
15	ILE	0	25	IP	1[2]
16	EE	0	26	IR	0
17	PR	0	27	DR	0
18	FP	0	28–29	—	Unspecified[1]
19	ME	0	30	RI	0
20	FE0	0	31	LE	0
21	SE	0			

Notes:
1. Unspecified can be either 0 or 1
2. 1 is typical, but might be 0

BAT Registers

Upper BAT Register

Bit(s)	Name	Description
0–14	BEPI	Block effective page index
15–18	—	Reserved
19–29	BL	Block length
30	Vs	Supervisor mode valid bit
31	Vp	User mode valid bit

Lower BAT Register

Bit(s)	Name	Description
0–14	BRPN	This field is used in conjunction with the BL field to generate high-order bits of the physical address of the block.
15–24	—	Reserved
25–28	WIMG	Memory/cache access mode bits W Write-through I Caching-inhibited M Memory coherence G Guarded
29	—	Reserved
30–31	PP	Protection bits for block

BAT Area Lengths

BAT Area Length	BL Encoding	BAT Area Length	BL Encoding
128 Kbytes	000 0000 0000	8 Mbytes	000 0011 1111
256 Kbytes	000 0000 0001	16 Mbytes	000 0111 1111
512 Kbytes	000 0000 0011	32 Mbytes	000 1111 1111
1 Mbyte	000 0000 0111	64 Mbytes	001 1111 1111
2 Mbytes	000 0000 1111	128 Mbytes	011 1111 1111
4 Mbytes	000 0001 1111	256 Mbytes	111 1111 1111

Name	0	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
orcx	31	S				A						B				412											Rc
ori	24	S				A						UIMM															
oris	25	S				A						UIMM															
rfi [1]	19	00000				00000						00000				50											0
rlwimix	20	S				A						SH				MB				ME							Rc
rlwinmx	21	S				A						SH				MB				ME							Rc
rlwnmx	23	S				A						B				MB				ME							Rc
sc	17	00000				00000						00000000000000														1	0
slwx	31	S				A						B				24											Rc
srawx	31	S				A						B				792											Rc
srawix	31	S				A						SH				824											Rc
srwx	31	S				A						B				536											Rc
stb	38	S				A						d															
stbu	39	S				A						d															
stbux	31	S				A						B				247											0
stbx	31	S				A						B				215											0
stfd	54	S				A						d															
stfdu	55	S				A						d															
stfdux	31	S				A						B				759											0
stfdx	31	S				A						B				727											0
stfiwx [4]	31	S				A						B				983											0
stfs	52	S				A						d															
stfsu	53	S				A						d															
stfsux	31	S				A						B				695											0
stfsx	31	S				A						B				663											0
sth	44	S				A						d															
sthbrx	31	S				A						B				918											0
sthu	45	S				A						d															
sthux	31	S				A						B				439											0
sthx	31	S				A						B				407											0
stmw [3]	47	S				A						d															
stswi [3]	31	S				A						NB				725											0
stswx [3]	31	S				A						B				661											0
stw	36	S				A						d															
stwbrx	31	S				A						B				662											0
stwcx.	31	S				A						B				150											1
stwu	37	S				A						d															
stwux	31	S				A						B				183											0
stwx	31	S				A						B				151											0
subfx	31	D				A						B			OE	40											Rc
subfcx	31	D				A						B			OE	8											Rc
subfex	31	D				A						B			OE	136											Rc
subfic	08	D				A						SIMM															
subfmex	31	D				A						00000			OE	232											Rc
subfzex	31	D				A						00000			OE	200											Rc
sync	31	00000				00000						00000				598											0
tlbia [1,4]	31	00000				00000						00000				370											0
tlbie [1,4]	31	00000				00000						B				306											0
tlbsync [1,4]	31	00000				00000						00000				566											0
tw	31	TO				A						B				4											0
twi	03	TO				A						SIMM															
xorx	31	S				A						B				316											Rc
xori	26	S				A						UIMM															
xoris	27	S				A						UIMM															

[1] Supervisor-level instruction
[2] Supervisor- and user-level instruction
[3] Load and store string or multiple instruction
[4] Optional instruction
[5] 32-bit instruction only

Memory Management Registers

Instruction BAT Registers		Data BAT Registers	
IBAT0U	SPR 528	DBAT0U	SPR 536
IBAT0L	SPR 529	DBAT0L	SPR 537
IBAT1U	SPR 530	DBAT1U	SPR 538
IBAT1L	SPR 531	DBAT1L	SPR 539
IBAT2U	SPR 532	DBAT2U	SPR 540
IBAT2L	SPR 533	DBAT2L	SPR 541
IBAT3U	SPR 534	DBAT3U	SPR 542
IBAT3L	SPR 535	DBAT3L	SPR 543

Encodings for the Branch Options Field

BO	Description
0000*y*	Decrement the CTR, then branch if the decremented CTR ≠ 0 and the condition is FALSE.
0001*y*	Decrement the CTR, then branch if the decremented CTR = 0 and the condition is FALSE.
001*zy*	Branch if the condition is FALSE.
0100*y*	Decrement the CTR, then branch if the decremented CTR ≠ 0 and the condition is TRUE.
0101*y*	Decrement the CTR, then branch if the decremented CTR = 0 and the condition is TRUE.
011*zy*	Branch if the condition is TRUE.
1*z*00*y*	Decrement the CTR, then branch if the decremented CTR ≠ 0.
1*z*01*y*	Decrement the CTR, then branch if the decremented CTR = 0.
1*z*1*zz*	Branch always.

Notes:

The *z* indicates a bit that is ignored. The *z* bits should be cleared to zero, as they may be assigned a meaning in some future version of the PowerPC architecture. The *y* bit provides a hint about whether a conditional branch is likely to be taken and is used by some PowerPC implementations to improve performance. Other implementations may ignore the *y* bit.

MSR Bit Settings

Bit(s)	Name	Description
0	—	Reserved. Full function.*
1–4	—	Reserved. Partial function.*
5–9	—	Reserved. Full function.
10–12	—	Reserved. Partial function.
13	POW	Power management enable 0 Power management disabled (normal operation mode). 1 Power management enabled (reduced power mode).
Note: Power management functions are implementation-dependent. If the function is not implemented, this bit is treated as reserved.		
14	—	Reserved—Implementation-specific
15	ILE	Exception little-endian mode. When an exception occurs, this bit is copied into MSR[LE] to select the endian mode for the context established by the exception.
16	EE	External interrupt enable 0 While the bit is cleared the processor delays recognition of external interrupts and decrementer exception conditions. 1 The processor is enabled to take an external interrupt or the decrementer exception.
17	PR	Privilege level 0 The processor can execute both user- and supervisor-level instructions. 1 The processor can only execute user-level instructions.
18	FP	Floating-point available 0 The processor prevents dispatch of floating-point instructions, including floating-point loads, stores, and moves. 1 The processor can execute floating-point instructions.
19	ME	Machine check enable 0 Machine check exceptions are disabled. 1 Machine check exceptions are enabled.
20	FE0	Floating-point exception mode 0
21	SE	Single-step trace enable (Optional) 0 The processor executes instructions normally. 1 The processor generates a single-step trace exception upon the successful execution of the next instruction.
Note: If the function is not implemented, this bit is treated as reserved.		
22	BE	Branch trace enable (Optional) 0 The processor executes branch instructions normally. 1 The processor generates a branch trace exception after completing the execution of a branch instruction, regardless of whether or not the branch was taken.
Note: If the function is not implemented, this bit is treated as reserved.		

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SA14–2093–00 **MPCPRGREF/D**

1ATX35209–0 PRINTED IN USA 8/96 IMPERIAL LITHO 23784 5,000 RISC YGAHAA