

A large, detailed wireframe model of a particle accelerator ring, likely the FAIR facility, is the central focus of the slide. The ring is composed of many parallel lines, creating a mesh-like structure. It is shown in a perspective view, curving around the page. In the background, there are faint, semi-transparent images of scientific equipment and diagrams, including what looks like a particle detector or a similar complex structure.

# **FESA Real-Time Performance**

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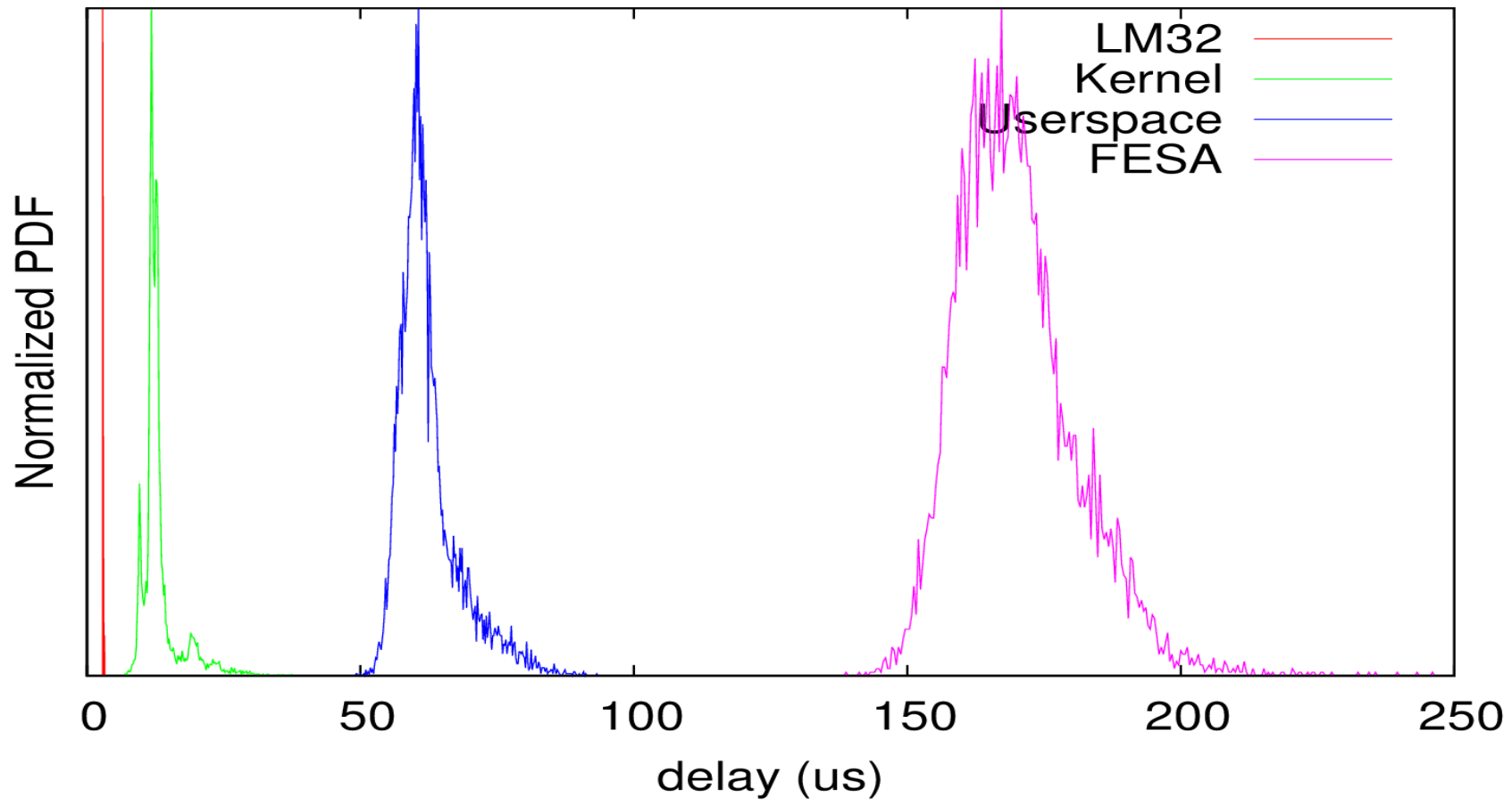
*from CS-CO-TG*

*<http://bel.gsi.de>*

# Timing requirements for FAIR

- To control FIP cards, need jitter  $< 20\mu\text{s}$
- To control kickers, need jitter  $< 3\text{ns}$
- Data master needs delay  $< 200\mu\text{s}$

# Timing Probability Density Function



# Actual delays, tabular

$\mu\text{s}$	Avg	StdDev	Max	Jitter
FPGA	0.001	0.001	0.001	0.001
LM32	2.924	0.058	3.217	0.354
Kernel	13.29	3.49	37.73	30.61
User	62.49	5.62	93.33	43.97
FESA	170.7	10.8	246.1	107.2

# What can be done?

- Don't use Linux for FESA
- Heavily optimize FESA timing performance

**OR**

- Do not use FESA to directly control output
- Use FESA to setup hardware to perform output

# Questions?



# Measurement

Linux 2.6.33.6 with real time patches

- CPU scaling was disabled (causes >200us delay to IRQs)
- CPU S states were disabled (causes >10us delay to IRQs)
- IRQ and tasklet RT priorities set to 99 (otherwise worse jitter)
- User process set to 98
- FESA set to 60

Oscilloscope (LeCroy WaveRunner 600MHz) measured gap of

- Output 1 = raised at same time as Interrupt from FPGA
- Output 2 = raised by software